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File 348:EUROPEAN PATENTS 1978-2004/Mar W02
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File 349:PCT FULLTEXT 1979-2002/UB=20040318,UT=20040311
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	Items	Description
S1	18269	(LEAST OR LESS OR LESSER OR SMALLEST OR SMALLER OR LOW???)-(1W)SIGNIFICAN??
S2	26031	(MOST OR GREATEST OR LARGEST OR HIGH???)(1W)SIGNIFICAN??
S3	3972	S1(10N)S2
S4	54657	(NUMBER? ? OR NUMERAL? ?)(5N)(SPLIT???? OR DIVIDE? ? OR DIVIDING OR BREAK??? OR BROKEN OR SEPARATE? ? OR SEPARATION OR -CHOP???? OR CARV???)
S5	11	S3(7N)S4

5/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00787632
Method for memorizing membership functions and the related circuit for calculating the grade of membership of the antecedents of fuzzy rules
Verfahren zur Speicherung von Zugehorigkeitsfunktionen und verwandte Schaltung zum Berechnen vom Zugehorigkeitsgrad der Vorbedingungen von Fuzzy-Regeln
Methode pour memoriser des fonctions d'appartenance et son circuit correspondantpour calculer le degre d'appartenance des antecedents des regles floues
PATENT ASSIGNEE:
Consorzio per la Ricerca sulla Microelettronica nel Mezzogiorno - CoRiMMe , (1176170), Stradale Primosole, 50, 95121 Catania, (IT), (Proprietor designated states: all)
INVENTOR:
Pappalardo, Francesco, Via G.B. Nicolosi 59, I-95047 Paterno'(Catania), (IT)
Matranga, Vincenzo, Via Empedocle Restivo 4, I-90144 Palermo, (IT)
Tesi, Davide, Via Fosso Secco 18/B, I-50010 Campi Bisenzio (Firenze), (IT)
Di Bella, Dario, Via Laudani 1, I-95030 Nicolosi (Catania), (IT)
LEGAL REPRESENTATIVE:
Modiano, Guido, Dr.-Ing. et al (40782), Modiano & Associati SpA Via Meravigli, 16, 20123 Milano, (IT)
PATENT (CC, No, Kind, Date): EP 735458 A1 961002 (Basic)
EP 735458 B1 010523
APPLICATION (CC, No, Date): EP 95830113 950328;
PRIORITY (CC, No, Date): EP 95830113 950328
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: G06F-007/00; G06F-007/48
ABSTRACT WORD COUNT: 207
NOTE:
Figure number on first page: 3

LANGUAGE (Publication,Procedural,Application): English; English; Italian
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	2772
CLAIMS B	(English)	200121	334
CLAIMS B	(German)	200121	287
CLAIMS B	(French)	200121	320
SPEC A	(English)	EPAB96	7703
SPEC B	(English)	200121	7493
Total word count - document A			10477
Total word count - document B			8434
Total word count - documents A + B			18911

...CLAIMS it comprises:
a register that contains the binary number to be divided;
an adder that receives, in a first input, the bits of said binary **number** to be **divided** , minus the n **least** **significant** bits and, in a second input, the **most** **significant** bit of said n **less** **significant** bits. ...

5/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00776111
Texturing and shading 3-D images
3-D-Bildertexturierung und -schattierung
Texturation et ombrage d'images 3-D
PATENT ASSIGNEE:
Imagination Technologies Limited, (1655302), Home Park Estate, Kings

Langley, Hertfordshire WD4 8LX, (GB), (Proprietor designated states: all)
INVENTOR:
Fenney, Simon J., 5 Ponsbourne Manor, Newgate, Street Village, Hertfordshire SG13 8QR, (GB)
Overliese, Ian J., 211 Ashmore Road, Queens Park, London W9 3DB, (GB)
Yassaie, Hossein, 111 Berekeley Avenue, Chesham, Buckinghamshire, HP5 2RS, (GB)
Dunn, Mark E., 26 The Ridgeway, Watford, Hertfordshire WD1 3TN, (GB)
Leaback, Peter D., 5 Links Drive, Radlett, WD7 3TN, (GB)
LEGAL REPRESENTATIVE:
Robson, Aidan John (69471), Reddie & Grose 16 Theobalds Road, London WC1X 8PL, (GB)
PATENT (CC, No, Kind, Date): EP 725366 A2 960807 (Basic)
EP 725366 A3 961106
EP 725366 B1 000920
APPLICATION (CC, No, Date): EP 96300622 960130;
PRIORITY (CC, No, Date): GB 9501832 950131
DESIGNATED STATES: DE; ES; FR; IT
INTERNATIONAL PATENT CLASS: G06T-015/10
ABSTRACT WORD COUNT: 287
NOTE:
Figure number on first page: NONE

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200038	319
CLAIMS B	(German)	200038	302
CLAIMS B	(French)	200038	400
SPEC B	(English)	200038	7319
Total word count - document A			0
Total word count - document B			8340
Total word count - documents A + B			8340

5/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00646563
Arrangement for recording or reproducing data reduced video information
Anordnung zur Aufzeichnung und Wiedergabe von datenreduzierter Videoinformation
Arrangement pour l'enregistrement et la reproduction d'informations video comprimees
PATENT ASSIGNEE:
Koninklijke Philips Electronics N.V., (1489041), Groenewoudseweg 1, 5621 BA Eindhoven, (NL), (applicant designated states: AT;DE;FR;GB)
INVENTOR:
Rijckaert, Albert Maria Arnold, c/o Int. Octrooibureau B.V., Prof.Holstlaan 6, NL-5656 AA Eindhoven, (NL)
Persoon, Eric Hendrik Jozef, c/o Int. Octrooibureau B.V., Prof.Holstlaan 6, NL-5656 AA Eindhoven, (NL)
van Gestel, Wilhelmus Jacobus, c/o Int. Octrooibureau B.V., Prof.Holstlaan 6, NL-5656 AA Eindhoven, (NL)
De With, Peter Hendrik Nelis, c/o Int. Octrooibureau B.V., Prof.Holstlaan 6, NL-5656 AA Eindhoven, (NL)
LEGAL REPRESENTATIVE:
van der Kruk, Willem Leonardus et al (51131), INTERNATIONAAL OCTROOIBUREAU B.V., Prof. Holstlaan 6, 5656 AA Eindhoven, (NL)
PATENT (CC, No, Kind, Date): EP 624991 A2 941117 (Basic)
EP 624991 A3 950614
EP 624991 B1 990804
APPLICATION (CC, No, Date): EP 94201317 940510;
PRIORITY (CC, No, Date): EP 93201392 930514
DESIGNATED STATES: AT; DE; FR; GB
INTERNATIONAL PATENT CLASS: H04N-009/80;

ABSTRACT WORD COUNT: 210

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9931	2181
CLAIMS B	(German)	9931	1916
CLAIMS B	(French)	9931	2548
SPEC B	(English)	9931	10800
Total word count - document A			0
Total word count - document B			17445
Total word count - documents A + B			17445

...CLAIMS word, a second packet portion comprising data reduced video information, each datablock defining a subpicture of a plurality of subpictures in which a picture is **divided** , a datablock comprising a **number** of n DC coefficients, a plurality of **most significant** AC coefficients and a plurality of **least significant** AC coefficients, where n is an integer for which holds that n>1, - data expansion means (206) for expanding data reduced video information included...

5/3,K/4 **(Item 4 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS
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00417884

Method and apparatus for performing mathematical functions using polynomial approximation and a rectangular aspect ratio multiplier

Verfahren und Gerat zur Ausfuhrung mathematischer Funktionen mit Hilfe polynomialer Annaherung und eines Multiplizierers rechteckigen Seitenverhaltnisses

Procede et appareil pour l'execution de fonctions arithmetiques en utilisant l'approximation polynomiale et un multiplieur a format rectangulaire

PATENT ASSIGNEE:
TEXAS INSTRUMENTS INCORPORATION, (1258120), 1761 International Parkway, Suite 135, Richardson, Texas 75081, (US), (applicant designated states: AT;BE;CH;DE;DK;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Brightman, Thomas B., 3509 O'Malley Court, Plano, Texas 75023, (US)
Ferguson, Warren, 3241 High Lark Dr., Dallas, Texas 75234, (US)
LEGAL REPRESENTATIVE:
UEXKULL & STOLBERG (100011), Patentanwalte Beselerstrasse 4, 22607 Hamburg, (DE)
PATENT (CC, No, Kind, Date): EP 421092 A2 910410 (Basic)
EP 421092 A3 920513
EP 421092 B1 990113
APPLICATION (CC, No, Date): EP 90115475 900810;
PRIORITY (CC, No, Date): US 416110 891002
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: G06F-007/544;
ABSTRACT WORD COUNT: 124

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9902	1704
CLAIMS B	(German)	9902	1757
CLAIMS B	(French)	9902	1945
SPEC B	(English)	9902	13356
Total word count - document A			0
Total word count - document B			18762
Total word count - documents A + B			18762

...SPECIFICATION provide for the truncation of leading bits.
An additional consideration results when it is necessary to not merely

truncate leading bits of a signed digit **number** , but actually **separate** the signed digit **number** into a **most significant** portion and a **least significant** portion without affecting the accuracy of each portion or incurring the speed penalties incurred in a conversion of the entire bit string to non-redundant...

5/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2004 European Patent Office. All rts. reserv.

00417682
Rectangular array signed digit multiplier.
Rechteckiger Matrixstrukturierter Vorzeichenziffernmultiplizierer.
Multiplieur pour des nombres a chiffres signes a structure matricielle rectangulaire.
PATENT ASSIGNEE:
CYRIX CORPORATION, (1258120), 1761 International Parkway, Suite 135, Richardson, Texas 75081, (US), (applicant designated states: AT;BE;CH;DE;DK;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Briggs, Willard Stuart, 2248 Roundrock, Carrollton, Texas 75007, (US)
Matula, David William, 9609 Robin Meadow Drive, Dallas, Texas 75243, (US)
LEGAL REPRESENTATIVE:
UEXKULL & STOLBERG Patentanwalte (100011), Beselerstrasse 4, W-2000 Hamburg 52, (DE)
PATENT (CC, No, Kind, Date): EP 416308 A2 910313 (Basic)
EP 416308 A3 920513
APPLICATION (CC, No, Date): EP 90115264 900809;
PRIORITY (CC, No, Date): US 402798 890905
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS: G06F-007/49;
ABSTRACT WORD COUNT: 181

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) EPABF1 1725
SPEC A (English) EPABF1 10170
Total word count - document A 11895
Total word count - document B 0
Total word count - documents A + B 11895

...SPECTFICATION provide for the truncation of leading bits.
An additional consideration results when it is necessary to not merely truncate leading bits of a signed digit **number** , but actually **separate** the signed digit **number** into a **most significant** portion and a **least significant** portion without affecting the accuracy of each portion or incurring the speed penalties incurred in a conversion of the entire bit string to non-redundant...

5/3,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00356102
Apparatus for determining if there is a loss of data during a shift operation.
Gerat um festzustellen, ob wahrend einer Verschiebungsoperation Daten in Verlust geraten.
Dispositif de determination s'il y a une perte de donnees pendant une operation de decalage.
PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Cook, Peter William, Route 4-Lakeside Road, Mount Kisco New York 10549,

(US)
Montoye, Robert Kevin, 6903 Mountain Trail, Austin Texas 78732, (US)
LEGAL REPRESENTATIVE:
Jost, Ottokarl, Dipl.-Ing. (6092), IBM Deutschland Informationssysteme GmbH, Patentwesen und Urheberrecht, D-70548 Stuttgart, (DE)
PATENT (CC, No, Kind, Date): EP 377845 A2 900718 (Basic)
EP 377845 A3 920513
EP 377845 B1 951004
APPLICATION (CC, No, Date): EP 89122989 891213;
PRIORITY (CC, No, Date): US 297639 890113
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-005/01; G06F-007/48;
ABSTRACT WORD COUNT: 95

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	1151
CLAIMS B	(English)	EPAB95	1134
CLAIMS B	(German)	EPAB95	1092
CLAIMS B	(French)	EPAB95	1285
SPEC A	(English)	EPABF1	4934
SPEC B	(English)	EPAB95	5394
Total word count - document A			6085
Total word count - document B			8905
Total word count - documents A + B			14990

...SPECIFICATION in which the minimum shift size is some power of 2, i.e., 2(sup(c). In this case the shift is envisioned as a **number** to be **divided** into three sub-fields; "a" **most significant** bits, "b" middle bits and "c" **least significant** bits. This extension is illustrated in Figs. 14A and 14B, which is similar to Fig. 4 except that all shift amounts are multiplied by 2...

...SPECIFICATION in which the minimum shift size is some power of 2, i.e., 2(sup(c). In this case the shift is envisioned as a **number** to be **divided** into three sub-fields; "a" **most significant** bits, "b" middle bits and "c" **least significant** bits. This extension is illustrated in Figs. 14A and 14B, which is similar to Fig. 4 except that all shift amounts are multiplied by 2...

5/3,K/7 **(Item 7 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

00305904
Digital-to-analog converter.
Digital-Analog-Wandler.
Convertisseur numerique-analogique.
PATENT ASSIGNEE:
N.V. Philips' Gloeilampenfabrieken, (200769), Groenewoudseweg 1, NL-5621 BA Eindhoven, (NL), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Pelgrom, Marcellinus Johannes Maria, c/o INT. OCTROOIBUREAU B.V. Prof. Holstlaan 6, NL-5656 AA Eindhoven, (NL)
Duinmaijer, Adrianus Cornelis Jozef, c/o INT. OCTROOIBUREAU B.V. Prof. Holstlaan 6, NL-5656 AA Eindhoven, (NL)
LEGAL REPRESENTATIVE:
van der Kruk, Willem Leonardus et al (51131), INTERNATIONAAL OCTROOIBUREAU B.V. Prof. Holstlaan 6, NL-5656 AA Eindhoven, (NL)
PATENT (CC, No, Kind, Date): EP 289081 A1 881102 (Basic)
EP 289081 B1 911218
APPLICATION (CC, No, Date): EP 88200749 880420;
PRIORITY (CC, No, Date): NL 87983 870427
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: H03M-001/74; H03M-001/80;
ABSTRACT WORD COUNT: 316

LANGUAGE (Publication,Procedural,Application): English; English; Dutch
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1140
CLAIMS B	(German)	EPBBF1	1023
CLAIMS B	(French)	EPBBF1	1252
SPEC B	(English)	EPBBF1	6280
Total word count - document A			0
Total word count - document B			9695
Total word count - documents A + B			9695

...SPECIFICATION the digital-to-analog converter may be further characterized in that M3=M5=M7=1, in that M8 is the value corresponding to the binary **number constituted** by the q **least significant** bits of the n- **bit digital** signal, M1 is the value corresponding to the binary number **constituted by** the n-p-q **most significant** bits and M4 is the value corresponding to the binary

5/3,K/8 (Item 8 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS
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00265235
Device for controlling address storing in a translation look-aside buffer.
Steuereinrichtung zur Speicherung von Adressen in einem Adressenubersetzungspufferspeicher.
Dispositif de commande de memorisation d'adresse dans une memoire tampon de traduction.
PATENT ASSIGNEE:
NEC CORPORATION, (236690), 7-1, Shiba 5-chome Minato-ku, Tokyo 108-01, (JP), (applicant designated states: BE;DE;FR;GB;IT;NL;SE)
INVENTOR:
Kinoshita, Kouji c/o NEC Corporation, 33-1, Shiba 5-chome, Minato-ku Tokyo, (JP)
LEGAL REPRESENTATIVE:
VOSSIUS & PARTNER (100311), Postfach 86 07 67, D-81634 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 275530 A2 880727 (Basic)
EP 275530 A3 900620
EP 275530 B1 930929
APPLICATION (CC, No, Date): EP 87119015 871222;
PRIORITY (CC, No, Date): JP 86307361 861223
DESIGNATED STATES: BE; DE; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: G06F-009/38; G06F-012/10;
ABSTRACT WORD COUNT: 142

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	618
CLAIMS B	(German)	EPBBF1	490
CLAIMS B	(French)	EPBBF1	634
SPEC B	(English)	EPBBF1	7683
Total word count - document A			0
Total word count - document B			9425
Total word count - documents A + B			9425

...SPECIFICATION in the request address register 35(') of twenty-five bits. In this connection, the request address signal also has twenty-five bits which can be **divided** into a **higher significant** part **of** eighteen bits and a **lower significant** part of seven bits.
The **higher significant** part of eighteen bits is produced as a first address signal of eighteen bits from the request address register 35(') through a first address signal...

5/3,K/9 (Item 9 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS
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00220498
Circuitry for complementing binary numbers.
Komplementierschaltung fur Binarzahlen.
Circuit de complementation de nombres binaires.
PATENT ASSIGNEE:
RCA LICENSING CORPORATION, (944400), 2 Independence Way, Princeton New Jersey 08540, (US), (applicant designated states: AT;DE;FR;GB;IT)
INVENTOR:
Christopher, Lauren Ann, 4 Eaton Place, Hopewell New Jersey, (US)
LEGAL REPRESENTATIVE:
[illegible], Richard Wilson et al (46454), London Patent Operation G.E. TECHNICAL SERVICES CO. INC. Burdett House 15/16 Buckingham Street, London WC2N 6DU, (GB)
PATENT (CC, No, Kind, Date): EP 209308 A2 870121 (Basic)
EP 209308 A3 880713
EP 209308 B1 911009
APPLICATION (CC, No, Date): EP 86305249 860708;
PRIORITY (CC, No, Date): US 755011 850715
DESIGNATED STATES: AT; DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: G06F-007/48; G06F-007/544; H03K-019/21; H03K-019/094;
ABSTRACT WORD COUNT: 227

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1149
CLAIMS B	(German)	EPBBF1	1114
CLAIMS B	(French)	EPBBF1	1278
SPEC B	(English)	EPBBF1	4605
Total word count - document A			0
Total word count - document B			8146
Total word count - documents A + B			8146

...SPECIFICATION may be complemented by simply inverting the sign bit. In ones complement notation the range of values which may be represented by an N-bit **number** is **divided** equally between **positive** and **negative** values. For positive **numbers** , the **most significant** bit (MSB) is **zero and** the N-1 **less significant** bits hold the **conventional binary** representation of the digital value. For negative numbers, however, the MSB is one and the N-1 less significant bits hold the bit-by-bit...

5/3,K/10 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00875830
SYSTEMS AND METHODS FOR TRANSMITTING DATA PACKETS
SYSTEMES ET PROCEDES DE TRANSMISSION DE PAQUETS DE DONNEES
Patent Applicant/Inventor:
HARIHARASUBRAHMANIAN Shrikumar, 1381 South East Street, Amherst, MA 01002 , US, US (Residence), IN (Nationality)
Legal Representative:
SNYDER Glenn (et al) (agent), Harrity & Snyder, L.L.P., Suite 300, 3900 North Fairfax Drive, Arlington, VA 22203, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200209370 A1 20020131 (WO 0209370)
Application: WO 2000US40576 20000804 (PCT/WO US0040576)
Priority Application: US 99147764 19990807
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 7323

Fulltext Availability:
Detailed Description

Detailed Description
... present invention. The sequence number field 600 may be divided into fields 610, 620 and 630. In alternative implementations of the present invention, the sequence **number** field 600 may be **divided** into different **numbers** of fields. Field 630 may represent the **least significant** bits and field 610 may represent the **most significant** bits of sequence number field 600. The size of fields 610, 620 and 630 may be based on a number of factors, such as the...

5/3,K/11 **(Item 2 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00862476 **Image available**
APPARATUS, METHODS AND COMPUTER PROGRAM PRODUCTS FOR PERFORMING HIGH SPEED DIVISION CALCULATIONS
APPAREIL, PROCEDES ET PRODUITS DE PROGRAMME D'ORDINATEUR PERMETTANT DE REALISER DES DIVISIONS A GRANDE VITESSE
Patent Applicant/Inventor:
PELTON Walter E, 3584 Lancelot Court, Fremont, CA 94536, US, US (Residence), US (Nationality)
[illegible]RIDGE K Walt, 28 Bassett Street, #231, San Jose, CA 95110, US, US (Residence), US (Nationality)
Legal Representative:
RANSOM W Kevin (et al) (agent), Alston & Bird LLP, Bank of America Plaza, Suite 4000, 101 South Tryon Street, Charlotte, NC 28280-4000, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200195090 A2-A3 20011213 (WO 0195090)
Application: WO 2001US18709 20010611 (PCT/WO US0118709)
Priority Application: US 2000210372 20000609
Designated States: AE AG AL AM AT AT (utility model) AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ CZ (utility model) DE DE (utility model) DK DK (utility model) DM DZ EC EE EE (utility model) ES FI FI (utility model) GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SK (utility model) SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 11487

Fulltext Availability:
Detailed Description

Detailed Description
... invention for calculating a reciprocal for a 32-bit number M. For this embodiment, the reciprocal, 1 /M, has an accuracy of 32 bits. The **number** M is **separated** into two **numbers** : X for the **most significant** 20 bits of M and A for the 12 **less significant** bits of M. This embodiment provides an approximate value for 1/M using an equation that approximates the reciprocal. The equation was derived as follows...

...invention for calculating a reciprocal for a 64-bit number M. For this

...embodiment, the reciprocal, 1 /M, has an aceuracy of 64 bits. The **number** M is **separated** into two **numbers** : X for the **most significant** 32 bits of M and A for the 32 **less significant** bits of M. This embodiment provides an approximate value for 1/M using the following equation that approximates the reciprocal.

1 /M @@<<X
A)2...

...invention for calculating a reciprocal for a 32-bit number M. For this embodiment, the reciprocal, 1/M, has an accuracy of 32 bits. The **number** M is **separated** into two **numbers** : X for the **most significant** 16 bits of M and A for the 16 **less significant** bits of M. This embodiment provides an approximate value for 1 /M using an equation that approximates the reciprocal. The equation was derived as follows...

...invention for calculating a reciprocal for a 64-bit number M. For this embodiment, the reciprocal, 1/M, has an aceuracy of 64 bits. The **number** M is **separated** into two **numbers** : X for the **most significant** 22 bits of M and A for the 44 **less significant** bits of M. The embodiment shown in Figure 5 uses substantially the same equations as those presented for the embodiment described in 5 Figure 4...

...present invention for calculating a reciprocal for a 64-bit number M. For this embodiment, the reciprocal, lIM, has an accuracy of 64 bits. The **number** M is **separated** into two **numbers** : X for the **most significant** 20 bits of M and A for the 44 **less significant** bits of M. This embodiment provides an approximate value for 1/M using the following equation that approximates the reciprocal.